REMARKS

Applicants will address each of the Examiner's rejections in the order in which they appear in the Office Action.

Claim Rejections - 35 USC §103

Claims 1-18

In the Office Action, the Examiner rejects Claims 1-18 under 35 USC §103(a) as being unpatentable over Masuda et al. (US 6,107,983) in view of Shinotsuka et al. (US 6,191,408). This rejection is respectfully traversed.

More specifically, independent Claim 1 is directed to a light-emitting device comprising a display portion comprising a plurality of pixels, a driver circuit, wherein all semiconductor elements in the display portion and the driver circuit are n-channel type semiconductor elements, and wherein each of the plurality of pixels comprises a light-emitting element.

In the Office Action, the Examiner contends that Matsuda discloses a liquid crystal display device with a substrate 111, which includes a driver circuit (201a, 201b, 301a, 301b) and TFTs (165) coupled with pixel electrodes (citing Fig. 2 in Matsuda) and a logic circuit section (215a) having two 2-input NAND gates NA1 and NA2 (citing Fig. 3 in Matsuda). The Examiner admits that Matsuda does not disclose all semiconductor elements being n-channel type semiconductor elements. The Examiner, however, contends that Shinotsuka discloses a photosensor signal processing apparatus having n-channel MOSs (Q1,Q2). While Applicants traverse this rejection, in order to advance the prosecution of this application, Applicants have amended Claim 1.

Applicants respectfully submit that Shinotsuka does not teach or suggest the feature of Claim 1 of "a display portion comprising a plurality of pixels," as Shinotsuka discloses an image sensor in

Figs. 1 and 2, which is not a display portion. Further, neither Matsuda nor Shinotsuka disclose of suggest the feature of independent Claim 1 of "wherein each of said plurality of pixels comprises a light-emitting element."

Applicants respectfully submit that Matsuda and Shinotsuka also fail to clearly teach the claimed feature "wherein **all** semiconductor elements in said pixel portion and said driver circuit are n-channel type semiconductor elements," as recited in independent claim 1 (emphasis added). The mere fact that Shinotsuka may show n-channel transistors is not sufficient to show the claimed limitation that all of the semiconductor elements in the pixel portion and the driver circuit must be n-channel type semiconductor elements.

As explained in the specification for the present application, this feature of the claimed invention is advantageous as "The number of the steps for fabricating p-channel semiconductor elements are reduced to simplify the process of manufacturing the light-emitting device and to enable the light-emitting device to be manufactured at a lower cost." See page 5, lns. 18-23.

Hence, it is respectfully submitted that independent Claim 1 is not disclosed or suggested by the cited references. For substantially the same reasons, Claims 2-4, 6-10, 12-18 are also not disclosed or suggested by the cited references.[1] Accordingly, it is respectfully requested that this rejection be withdrawn.

Claims 19-45

The Examiner also rejects Claims 19-45 under 35 USC §103(a) as being unpatentable over Matsuda in view of Shinotsuka and further in view of Lei (US 6,169,391). This rejection is also respectfully traversed.

[1] Claims 5 and 11 are being canceled herein without prejudice or disclaimer.

While Applicants traverse this rejection, in order to advance the prosecution of this application, Applicants have amended independent Claims 19, 24, 28, 32, 36 and 41 in a similar manner to the features discussed above for Claim 1.[2]

For similar reasons as those discussed above for the rejection of Claims 1-18, Claims 19-21, 23-25 and 27 are also not disclosed or suggested by the cited references (Lei merely being cited as allegedly disclosing a gate of transistor (51) connected to a drain of transistor 46 in Figs. 7 and 9).

With respect to Claims 28-45, Lei discloses that for Fig. 7 (cited by the Examiner in support of the rejection), transistor 51 is an N channel depletion mode MOSFET (Col. 4, lns. 34-37 of Lei). Lei further discloses that for Fig. 9 (also cited by the Examiner in support of the rejection), an N channel enhancement mode MOSFET is substituted for the N channel depletion mode MOSFET of the transistor 51 of Fig. 7 (Col. 5, lns. 22-26 of Lei). Hence, transistor 51 in Lei is either an N channel depletion mode MOSFET or an N channel enhancement mode MOSFET. However, for at least the reasons discussed above, Applicants respectfully submit that the cited references fail to disclose or suggest that all the semiconductor elements in the display portion and the driver circuits are n-channel type semiconductor elements, as in the rejected claims.

New Claims

Applicants are also adding new dependent Claims 46-51. These claims are allowable for at least the reasons discussed above for the independent claims. Accordingly, it is requested that these claims be allowed.

If any fee should be due for these claims, please charge our deposit account 50/1039.

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[2] Applicants are canceling Claims 22, 26, 30, 34, 39 and 44 without prejudice or disclaimer.

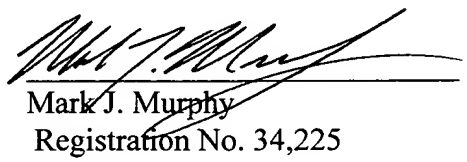
Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should now be allowed.

If any fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,



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